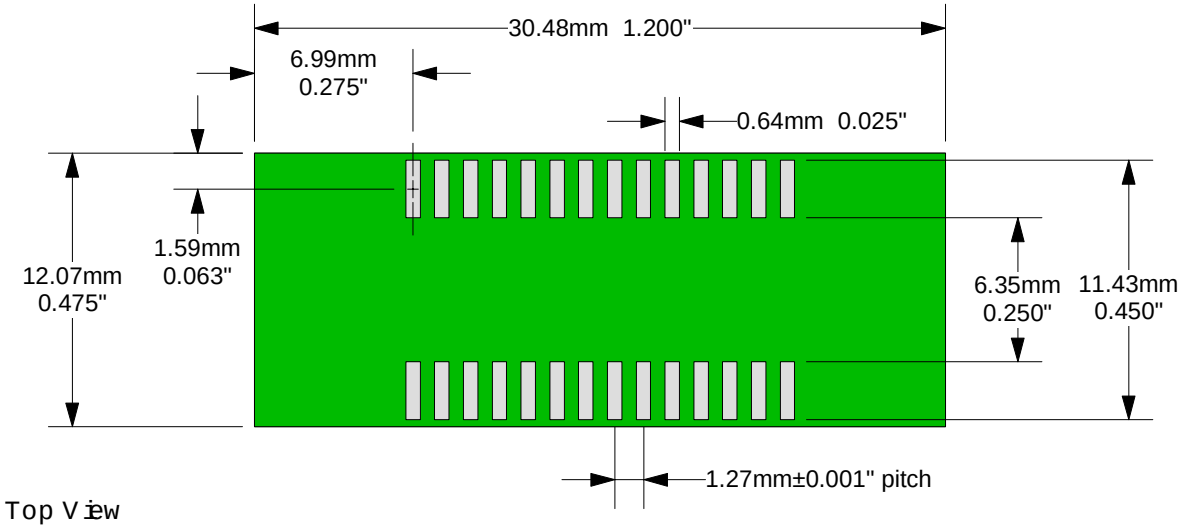
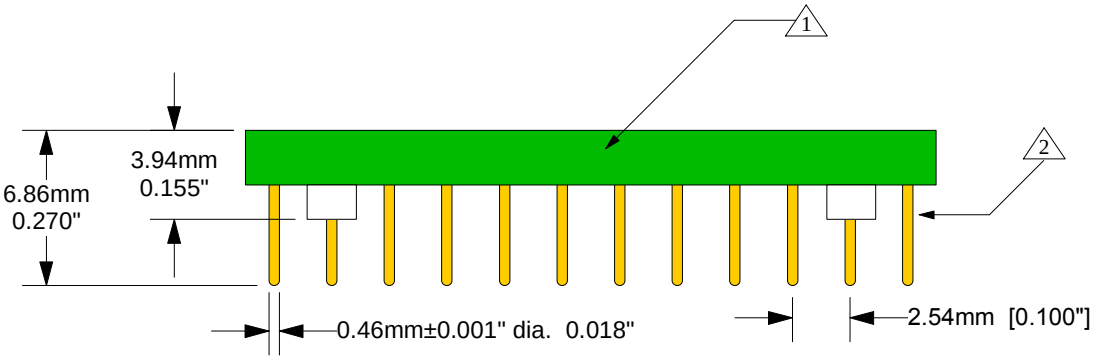
PIN MAPPING

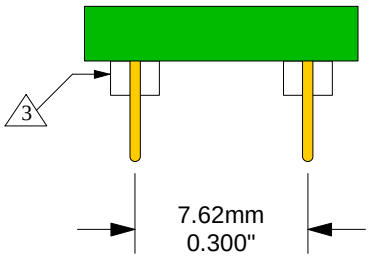
SO	DIP	Signal
1	1	LDACA
2	2	TFSA
3	3	DTA
4		NC
5	4	TCLKA
6	5	DGND
7	6	TP1
8	7	Vdd
9	8	AGND
10	9	Voutb
11		NC
12	10	Vss
13	11	TP2
14	12	REF INB
15	13	LDACB
16	14	TFSB
17	15	DTB
18		NC
19	16	TCLKB
20	17	DGND
21	18	TP3
22	19	Vdd
23	20	AGND
24	21	Vouta
25		NC
26	22	Vss
27	23	REF OUT
28	24	REF INA



Top View



Side View



End View

1. Substrate: 0.095"±0.007" FR4/G10 or equivalent high temp material. 1/2 oz. Cu clad. SnPb plating
2. Pins: Material- Brass Alloy 360 1/2 hard; finish- 10µ" Au over 50µ" Ni (min.).
3. Stand-off: material- Teflon; 0.085" Dia; 0.060" thick.

Description: SOIC to DIP Package Converter

28 position SOIC land pattern to 0.3" wide 24 pin DIP. Pin assignment: Analog Devices AD7242 to AD7244.

PC-SO/DIP-AD7244-01 Drawing	Status: Released	Scale: 3:1	Rev: A
 PO BOX 21151 ST. PAUL, MN 55121 Tele: (651) 452-8100 www.ironwoodelectronics.com	Drawing: M. Tully	Date: 12/8/00	
	File: PC-SO_DIP-AD7244-01 Dwg.mcd	Modified:	

Tolerances: diameters ±0.03mm [±0.001"],
PCB perimeters ±0.13mm [±0.005"],
PCB thicknesses ±0.18mm [±0.007"],
pitches (from true position) ±0.08mm [±0.003"],
all other tolerances ±0.13mm [±0.005"]
unless stated otherwise. Materials and specifications are subject to change without notice.