Multi Level Stacked Socket Challenges & Solutions

Mike Fedde, Ranjit Patil, Ila Pal & Vinayak Panavala
Ironwood Electronics

2010 BiTS Workshop
March 7 - 10, 2010
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According to Prismark, in 2020 - 3D packaging share of 7% might total well over 30 billion components that employ stacking technologies.
Multi Level IC Test Need

- Test processor by itself in a socket
- Test processor signals using a probe which is interfaced between processor and target PCB
- Test processor with memory soldered
- Test processor with replaceable memory
- Test memory signals using a probe which is interfaced between memory and processor
- Test memory signals and processor signals using memory probe and processor probe in the stack up between memory and processor on target PCB
Multi Level IC Socket Configuration

- Single level
  - Processor only

- Two level
  - Processor & Memory

- Single level
  - Processor + Memory Soldered

Socket assembly

Memory

Processor

Interposer
Multi Level IC Socket Configuration

Two level Processor & Memory probe

Three level Processor, Memory probe & Memory

Processor

Memory probe

Memory

Interposer

Socket assembly
Multi Level IC Socket Configuration

Single level
Processor soldered on probe

Two level
Processor & Processor probe

Socket assembly
Processor
Processor + Memory soldered
Processor probe
Interposer
Interposer

3/2010 Multi Level Stacked Socket – Challenges & Solutions
Multi Level IC Socket Configuration

Two level PoP & Processor probe

Three level Processor, Memory & Processor probe

- Socket assembly
- Memory
- Interposer
- Processor + Memory soldered
- Interposer
- Processor probe
- Interposer

8/2010 Multi Level Stacked Socket – Challenges & Solutions
Multi Level IC Socket Configuration

Three level
Memory soldered probe, Processor & Processor probe

Three level
Memory probe, Processor & Processor probe

Four level
Memory, Memory probe Processor & Processor probe

Three level
Memory soldered to Probe

Interposer

Processor

Interposer

Processor probe

Interposer

Socket assembly

Memory

Interposer

Memory probe

Interposer

Processor

Interposer

Processor probe

Interposer

Socket assembly

Memory

Interposer

Memory probe

Interposer

Processor

Interposer

Processor probe

Interposer

Multi Level Stacked Socket – Challenges & Solutions
Multi Level IC Socket Configuration

Socket assembly with 1st level elastomer interface

2nd level elastomer interface between memory & processor

Compression fixture for uniform force distribution
Multi Level IC Socket
Electrical Challenges

Source: Texas Instruments

Multi level socket with memory probe Interfaced to scope using high speed connectors
Multi Level IC Socket
Electrical Challenges

Four wing probe for DDR memory

Two wing probe for DDR memory under test

Two wing probe for DDR memory with optimized signal routing

Source: Agilent Technologies
Electrically Transparent Probing

Without interposer  With interposer

Source: Agilent Technologies
Multi Level Stack Up Alignment Challenges

Configuration 1: Processor and Memory
1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Memory will be centered on the Ball guide and IC guide.
Configuration 2: Processor and Memory Probe
1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Memory probe will be centered.
Multi Level Stack Up Alignment Challenges

Configuration 3: Processor, Probe board and Memory
1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Probe board will be centered.
3. PoP memory is shifted 0.25mm to left with IC guide and Ball guide.
Configuration 4: Processor Probe, Processor, Memory Probe and PoP

1. Processor and POP sits 0.25mm shifted with pattern on target board. Processor probe and memory probe sits centered with respect to target board.
2. Vertical elastomer on first layer.
Multi Level Stack Up
Alignment Challenges

Processor

Elastomer

Nominal contact area

Target board

IC guide

Ball guide

Elastomer guide

Alignment pin

0.0 4mm

0.1 1mm

0.4 0mm Pitch

Multi Level Stacked Socket – Challenges & Solutions
Multi Level Stack Up
Alignment Challenges

Processor/Elastomer/PCB tolerance : ±
PCB Alignment Hole position : +0.025mm
Ball guide Alignment Hole position : +0.025mm
PCB Pad location/Size : +0.05mm

=0.1mm off from nominal location

With 0.24mm minimum pad diameter for 0.4mm pitch BGA, elastomer contacts more than 58% of the pad. This XY variation occurs on each level of the stack up. Similar calculations were made for Z variations and manufacturing tolerances were updated such that 60% of pad is covered by elastomer.
Multi Level Stack Up
Force Challenges

Force balance using additional non-conductive rubber
Multi Level Stack Up
Force Challenges

- Force balance using angled interposer itself
- Shift allows normal force to be lower than vertical interposer
Multi Level Stack Up Force Challenges

• Force data for a four level interconnect stack up shown as per ball count
• Series network of forces are balanced at each level either by using an additional non-conductive rubber or elastomer by itself

<table>
<thead>
<tr>
<th></th>
<th>Elastomer</th>
<th>Ball Count</th>
<th>Force/Ball, gm</th>
<th>Total Force, Kg</th>
</tr>
</thead>
<tbody>
<tr>
<td>PoP</td>
<td>Angle</td>
<td>169</td>
<td>30</td>
<td>5.07</td>
</tr>
<tr>
<td>Memory Probe Processor</td>
<td>Angle</td>
<td>169</td>
<td>30</td>
<td>5.07</td>
</tr>
<tr>
<td>Processor</td>
<td>Angle</td>
<td>515</td>
<td>30</td>
<td>15.45</td>
</tr>
<tr>
<td>Processor Probe</td>
<td>Angle</td>
<td>515</td>
<td>35</td>
<td>18.025</td>
</tr>
<tr>
<td>Target Board</td>
<td>Straight</td>
<td>515</td>
<td>35</td>
<td></td>
</tr>
</tbody>
</table>
Conclusion

• 3D packages are the future
• Pitch, pin count, performance complexities increase due to consumer demand
• Two level package needs four level interconnect for development
• XYZ alignment challenges in each interconnect level push manufacturing capabilities to its extreme
• Force balancing at each level enables innovative design and requires new materials with unique properties