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Benefits of Signal Integrity (SI) Simulation for High Speed Sockets and Adapters.

Introduction

High-speed sockets and adapters continue to perform important functions for today's IC component and electronics packaging engineers. Whether for testing, prototyping, or production, these components typically require an ever-increasing level of electrical and mechanical performance. In the area of electrical performance, it is particularly important that an accurate predictive model be available for performance at GHz frequencies. Rather than relying solely upon historical measures derived from complex test configurations, these predictive models used in simulations are capable of providing accurate performance data in a timely as well as cost-effective manner. This data then serves as an aid to the design and test engineer relative to the initial selection of a proper interconnect design, and serve as a predictor of performance over a variety of simulated end-use conditions. Since a beneficial simulation technique must be both reliable and versatile, the goal of this paper is to demonstrate this utility across a wide range of interconnect product designs.

Background

Over the past several years, IC devices have continually increased in performance relative to both speed and functionality. These changes have been accompanied by new package styles featuring higher I/O counts with decreased spacing and reduced interconnect feature size. All of these factors combined create more demanding requirements upon the sockets and adapters used for interconnection.

At GHz level operating frequencies and beyond it has become increasingly important to understand the scattering and reflection properties of traveling waves when an interconnection network is inserted within a transmission line between an IC device and the attaching PC Board. S-parameter measurements in terms of reflection coefficients and transmission gain have typically been accomplished via the use of network and signal analyzers coupled with the use of special test fixtures and probing devices. Based on these measurements, network analysis provides the appropriate S-parameters from which impedance values may be derived and directly correlated via the use of Smith Charts.

Drawbacks to this traditional network analysis approach include the inability to probe within the center of an array for measurement data as well as the time and expense of performing such analysis. Computer-aided simulation offers an alternative approach to S-parameter derivation that is both timely and cost-effective. As a modeling technique,

simulation also provides the capability to generate data across a complete array of interconnection ports. A useful tool for this type of high-frequency simulation has proven to be the CST Microwave Studio™ offered by Computer Simulation Technology. The application of this technology to the simulation of high-speed interconnection sockets and adapters provide data that is accurate and reliable as well as adaptable to new designs of the future.

Comparison of Simulated and Experimental Results – GHz Socket

One type of high-speed socket interconnection media in use today utilizes conductive wires embedded within an elastomeric matrix (Figure 1). From a mechanical design perspective, this matrix of conductors has proven to meet the mechanical requirements regarding tolerance variations from package to PC board while also providing the compression characteristics for repeated use over time. From an electrical performance perspective, the modeling of this interface is shown in Figure 2 where the key parameters for modeling purposes become the conductivity, spacing, and length of the wire matrix along with the dielectric constant of the surrounding insulating material. Simulated insertion loss data from the modeling process is shown in Figure 3. Figure 4 provides further data from the simulation process displaying both return and crosstalk results (NEXT and FEXT). Figure 5 and figure 6 shows Smith Chart and VSWR respectively. Table 1 shows the translated appropriate inductance and capacitance results for these same data points.

0.5mm GHz BGA socket simulation data

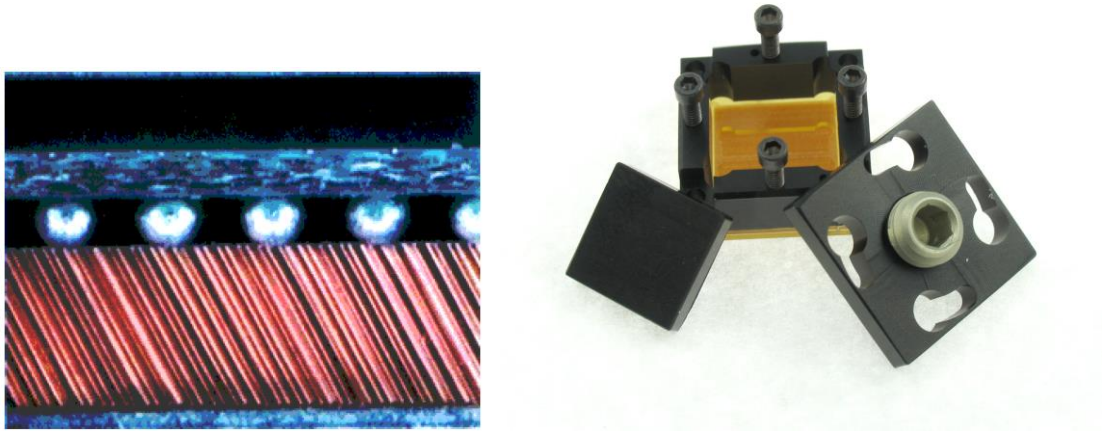

Figure 1 – BGA GHz socket with angled elastomeric interconnect

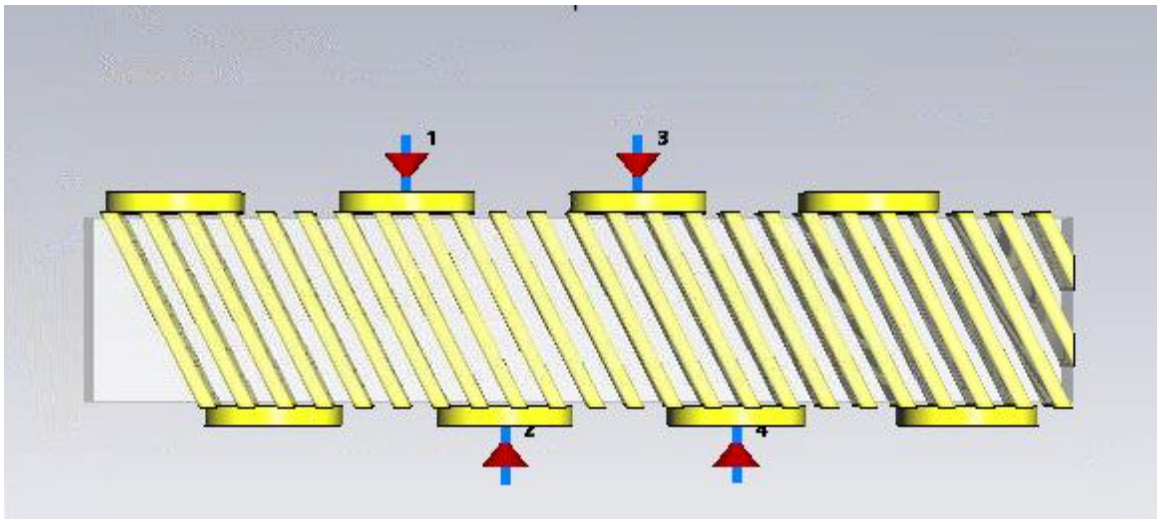

Figure 2a: Elastomeric interconnect simulation based on 4x4, 0.5mm pitch BGA array

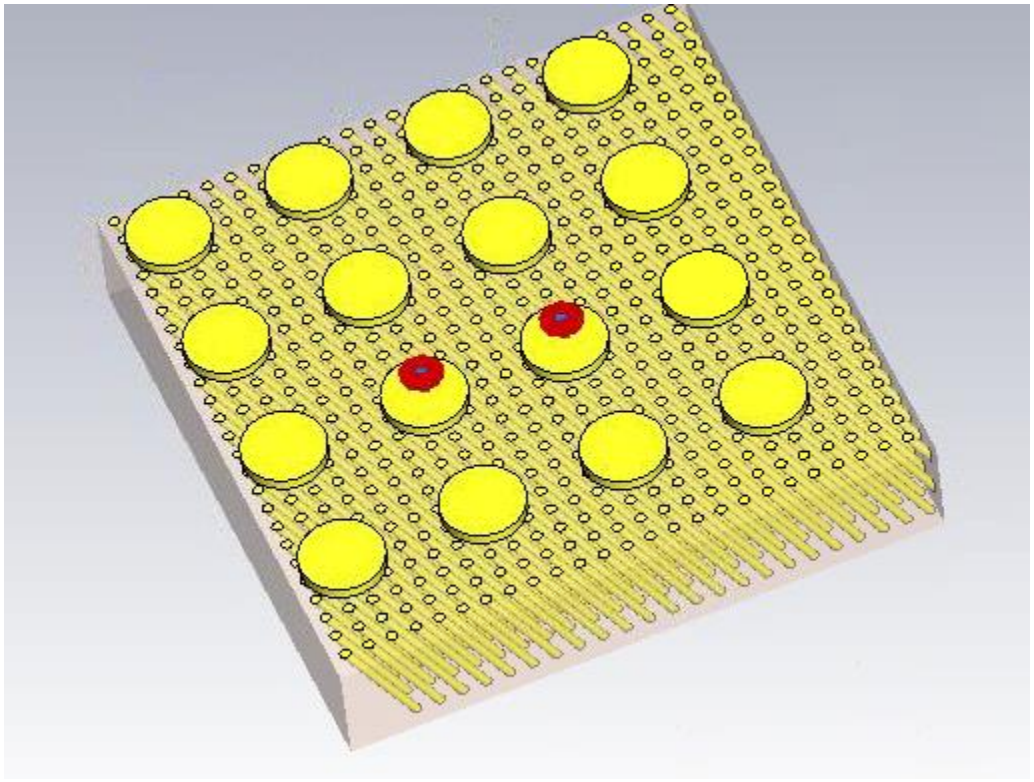

Figure 3b: Elastomeric interconnect simulation based on 4x4, 0.5mm pitch BGA array

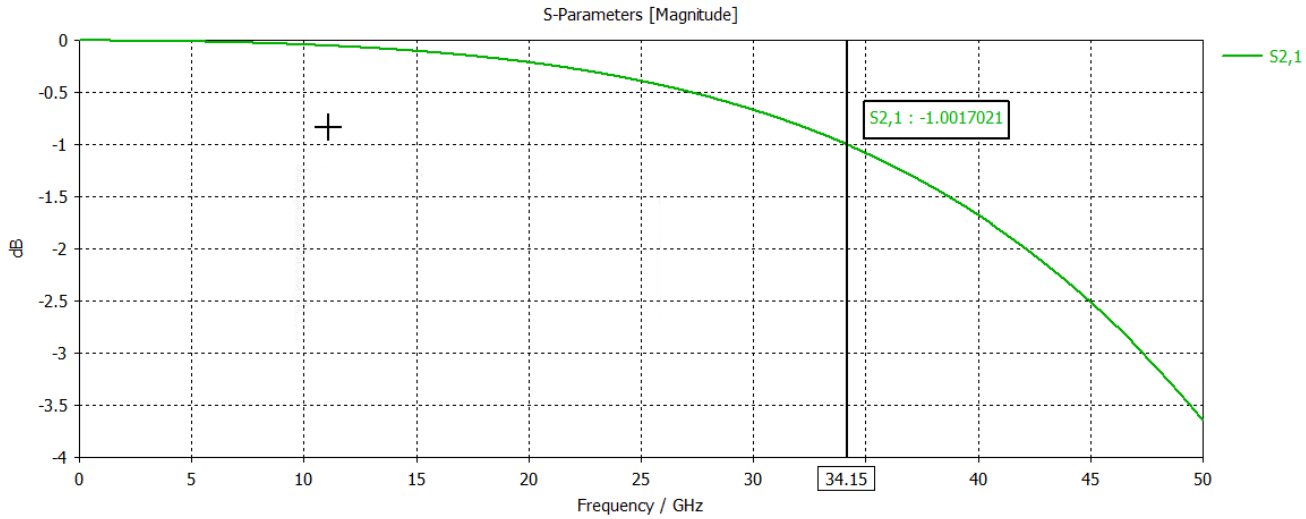

Figure 4: Simulated Insertion loss: Less than -1dB to > 34 GHz

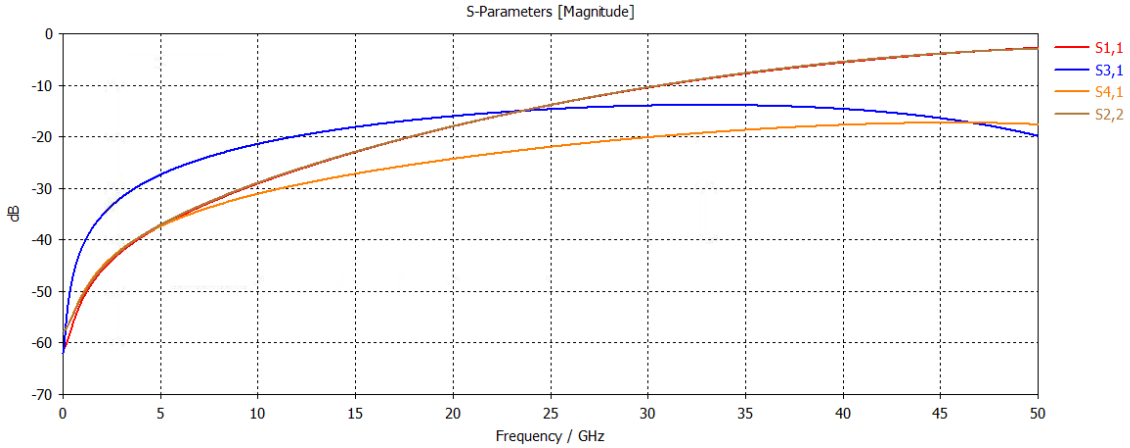

Figure 4: Simulated Return Loss and Crosstalk. S1_1 represents return loss at pin 1, S31 (NEXT) and S41 (FEXT)

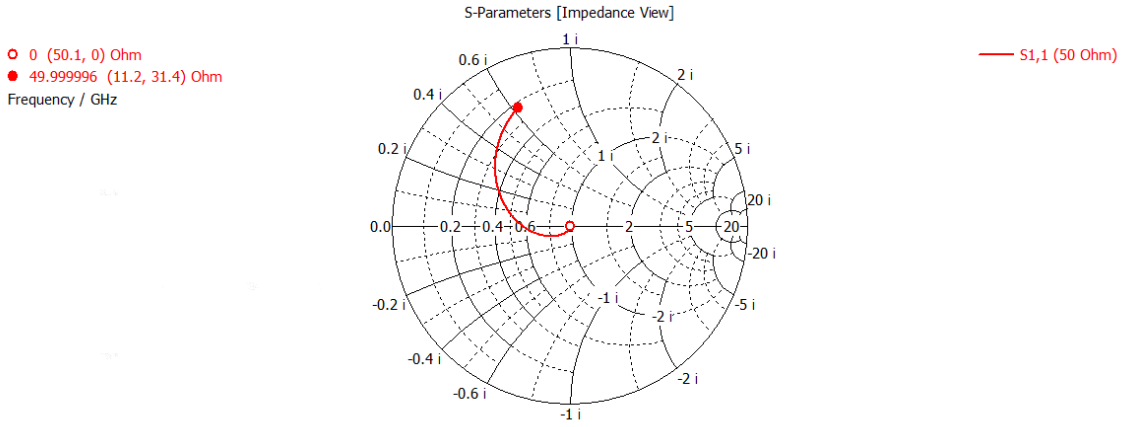

Figure 5: Smith Chart

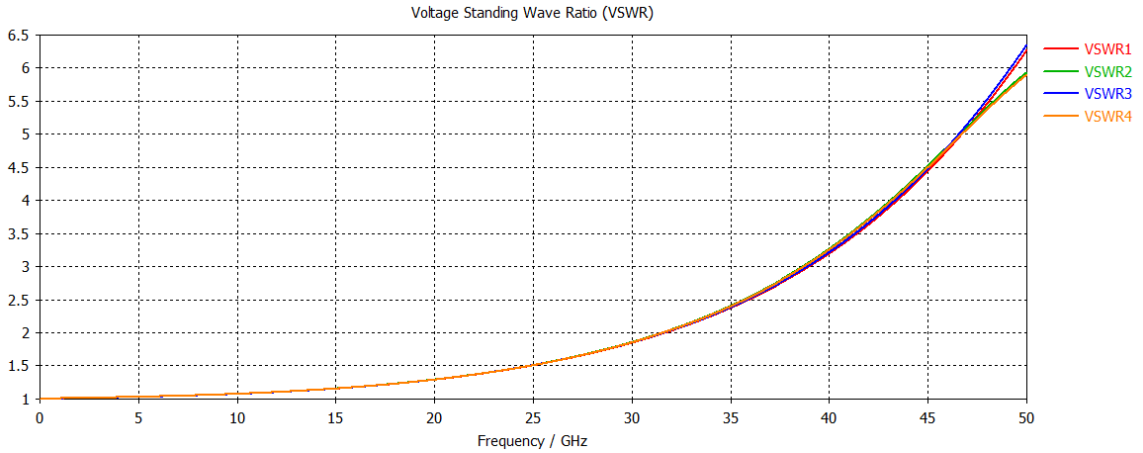

Figure 6: VSWR

Capacitance (pF) to GND for all pins (1-16): 0.5mm GHz BGA socket

0.0090	0.0052	0.0052	0.0090
0.0052	0.0049	0.0049	0.0052
0.0052	0.0049	0.0049	0.0052
0.0090	0.0052	0.0052	0.0090

Self-inductance (nH) of the pins (1-16): 0.5mm GHz BGA socket

0.0359	0.0516	0.0516	0.0359
0.0516	0.0595	0.0595	0.0516
0.0516	0.0595	0.0595	0.0516
0.0359	0.0516	0.0516	0.0359

Mutual inductance (nH) for some pins: 0.5mm GHz BGA socket

Pin1	L_{12}=0.0031	L_{13}=0.00053	L_{14}=0.000036
L_{56}=0.0065	Pin6	L_{67}=0.01713	L_{68}=0.00172
L_{911}=0.00173	L_{1011}=0.01719	Pin11	L_{1112}=0.0065
L_{1316}=0.000037	L_{1416}=0.00055	L_{1516}=0.00307	Pin16

Table 1 - GHz BGA socket capacitance and inductance data

Simulation Versatility for Alternative Interconnect Designs

Simulation capability has also proven to be versatile to its application for a variety of interconnect designs. Figure 1 depicts the application of EM modeling to a more traditional pin and socket interface. Spaced on 0.8 mm, the conductive elements in this design consist of gold-plated contacts contained within an insulating material of traditional FR-4 PC board material. Simulated insertion loss is less than -1db to 1.8 GHz shows useful range of this product for a variety of applications. Corresponding return loss and crosstalk (Figure 3), and electrical inductance and capacitance data (Table 1) are then provided. Additional simulation models have been developed for two additional designs. Figure 4 depicts a spring pin design with corresponding insertion loss shown in Figure 5, return loss and crosstalk shown in Figure 6. Figure 7 depicts an adapter for a QFN package with corresponding insertion loss data shown in Figure 8, return loss and crosstalk shown in Figure 9. More detailed results in terms of crosstalk, return loss, and impedance values are available for these designs as well.

Giga-snaP™ adapter simulation data

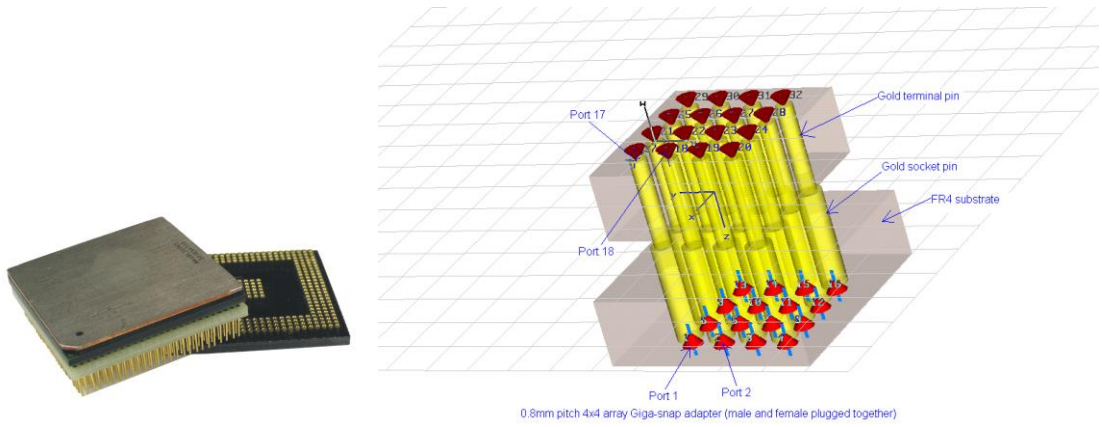

Figure 1: Giga-snaP™ adapter model based on 4x4, 0.8mm pitch BGA array

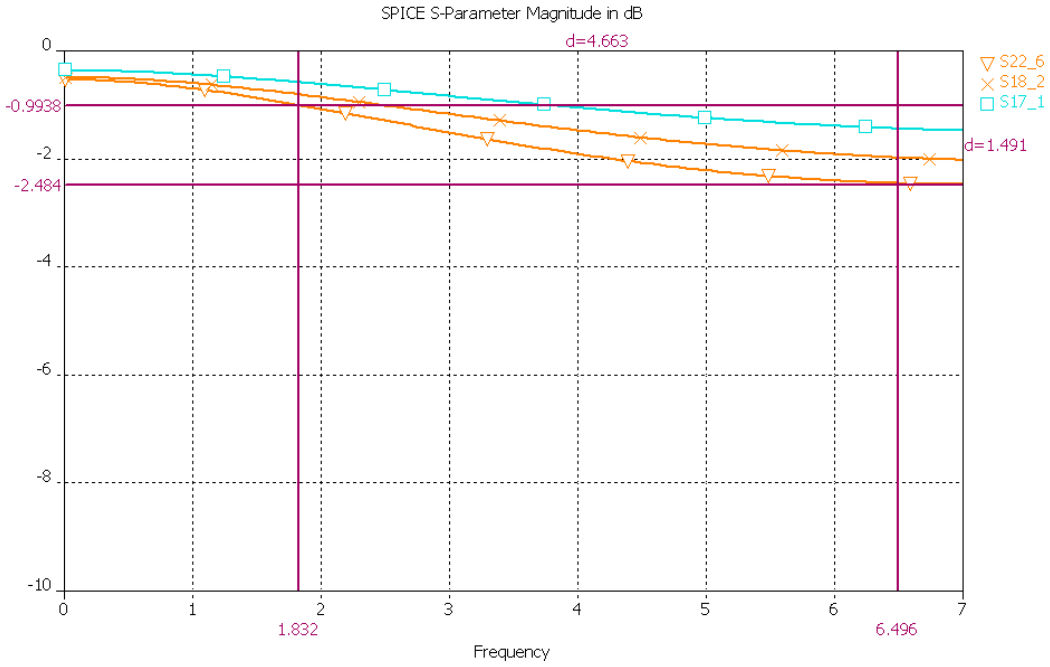

Figure 2: Simulated Insertion loss: Less than -1dB to 1.8GHz

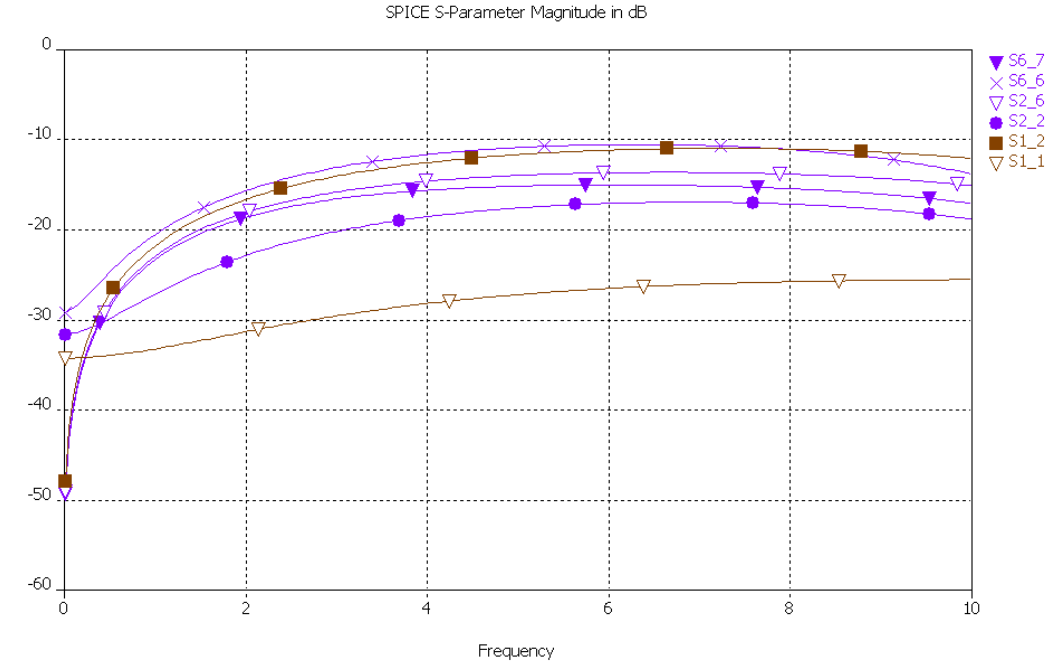

Figure 3: Simulated Return Loss and Crosstalk. S1_1 represents return loss at pin 1, S2_6 represents crosstalk between pin 2 and pin 6.

Capacitance (pF) to GND for all pins (1-16): Giga-snaP™ adapter

0.2397	0.1080	0.1080	0.2397
0.1080	0.0054	0.0054	0.1080
0.1080	0.0054	0.0054	0.1080
0.2397	0.1080	0.1080	0.2397

Self-inductance (nH) of the pins (1-16): Giga-snaP™ adapter

1.5894	1.5798	1.5798	1.5894
1.5798	1.569	1.569	1.5798
1.5798	1.569	1.569	1.5798
1.5894	1.5798	1.5798	1.5894

Mutual inductance (nH) for some pins: Giga-snaP™ adapter

Pin1	L_{12}=0.6412	L_{13}=0.3188	L_{14}=0.1666
L_{56}=0.6532	Pin6	L_{67}=0.6509	L_{68}=0.3455
L_{911}=0.3455	L_{1011}=0.6509	Pin11	L_{1112}=0.6532
L_{1316}=0.1665	L_{1416}=0.3188	L_{1516}=0.6412	Pin16

Table 1 – Giga-snaP™ adapter capacitance and inductance data

Spring Pin socket simulation data

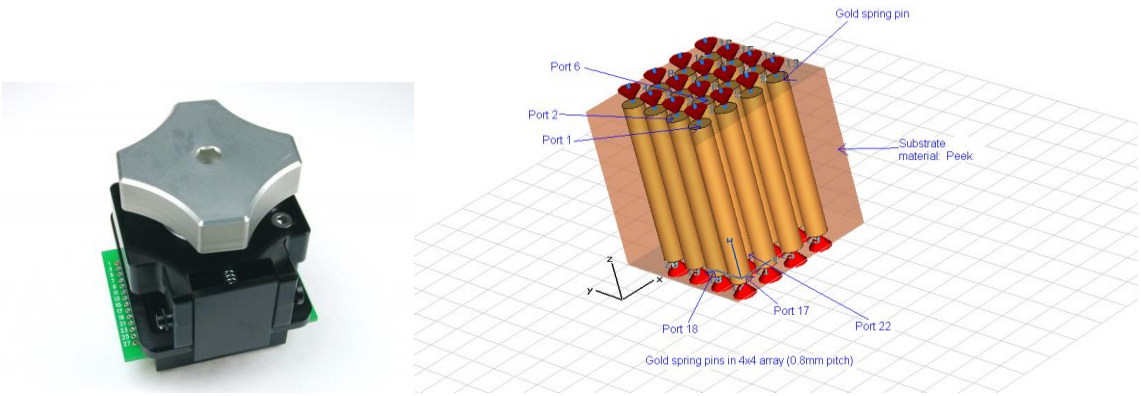

Figure 4: Spring Pin model based on 4x4, 0.8mm pitch BGA array

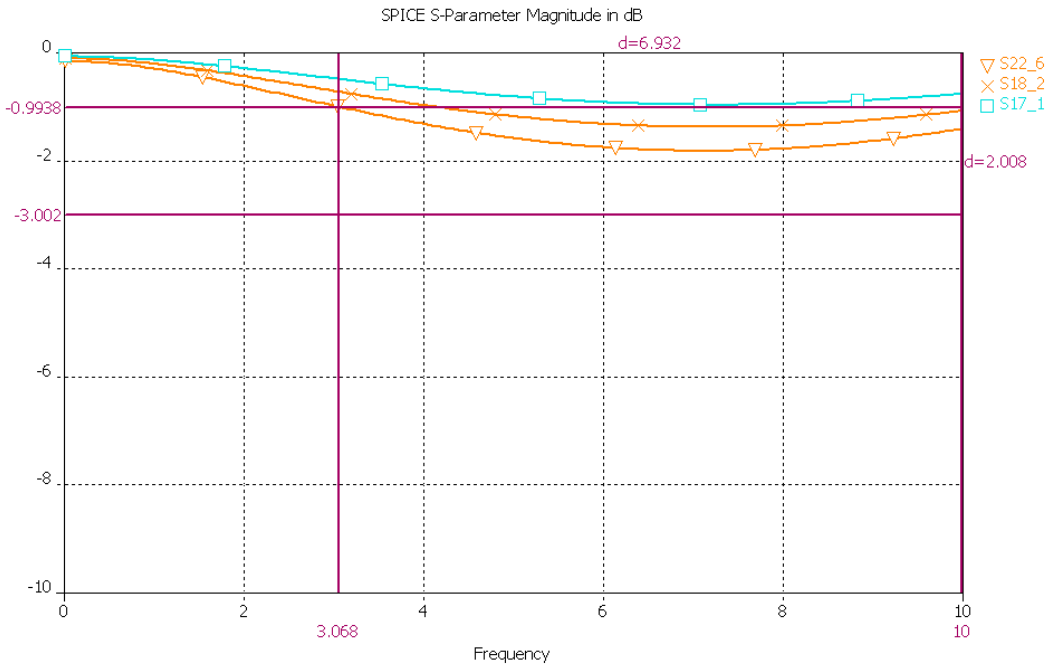

Figure 5: Simulated Insertion loss: Less than -1dB to 3.0GHz

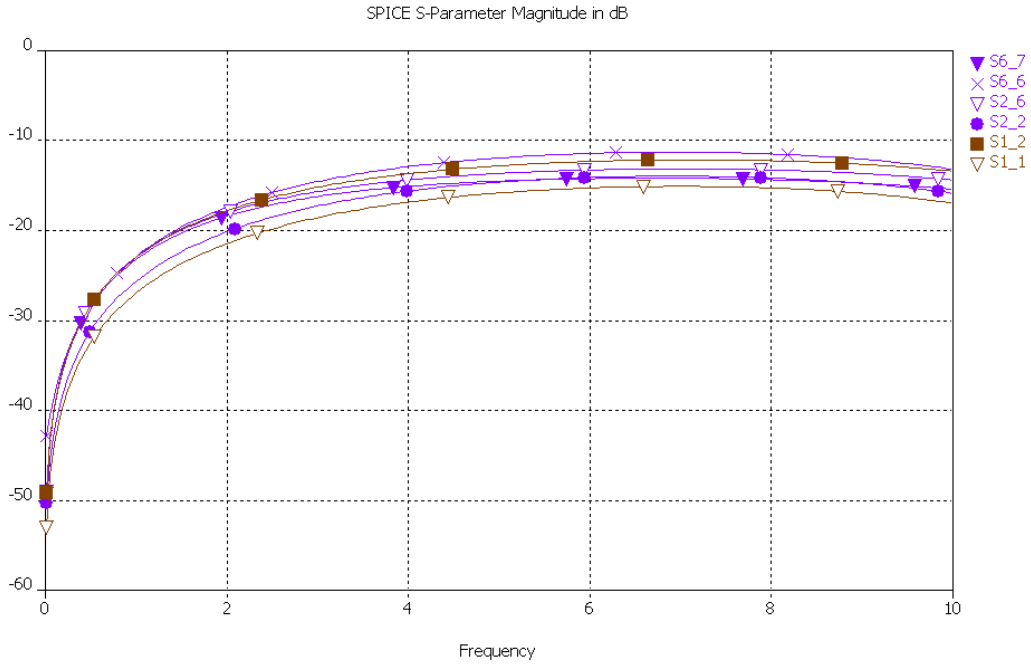

Figure 6: Simulated Return loss and Crosstalk. S1_1 represents return loss at pin 1, S2-6 represents crosstalk between pin 2 and pin 6.

QFN Adapter simulation data

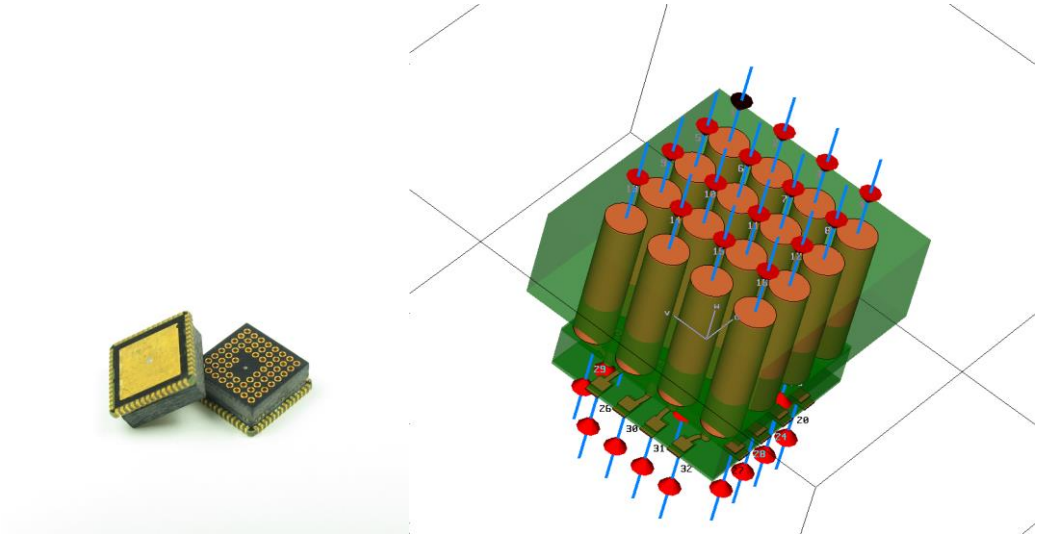

Figure 7: QFN adapter model based on 16 position to 4x4 array on 0.8mm pitch

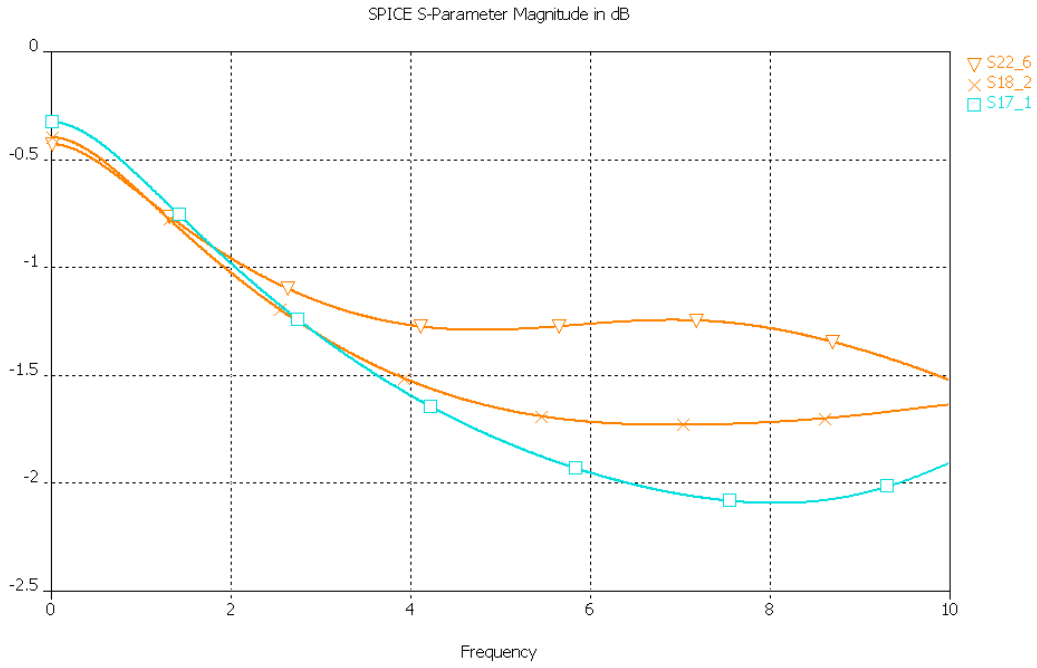

Figure 8: Simulated Insertion loss: Less than -1dB at to 1.9 GHz

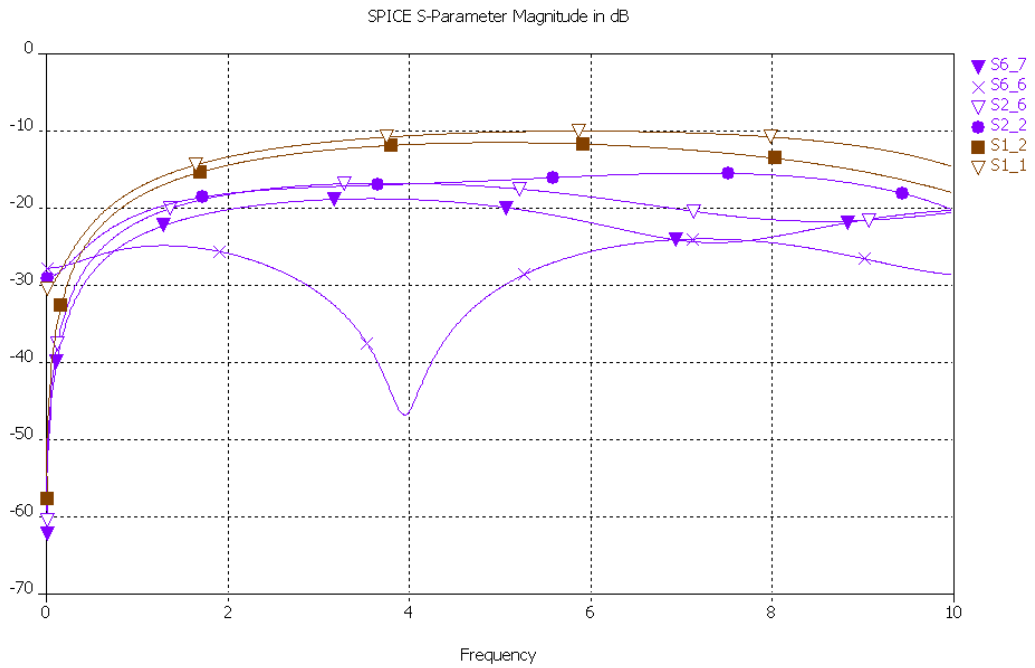

Figure 9: Simulated Return loss and Crosstalk. S1_1 represents return loss at pin 1, S2_6 represents crosstalk between pin 2 and pin 6.

Conclusion

Electromagnetic simulation modeling capability has proven to be an efficient and effective means for the interconnection provider to keep pace with the rapidly changing world of high-speed microelectronic device testing, prototyping, and end-product applications. Ironwood Electronics, Inc. uses CST Studio Suite® simulation tool to extract SI properties of several different socket and adapter product families and they are available upon request. This paper demonstrates both accuracy and versatility of SI simulation technique.

About Ironwood Electronics

Ironwood Electronics Inc. designs and manufactures prototype and production adapters and high-speed sockets for semiconductor industry.

www.ironwoodelectronics.com

About CST Studio Suite®

CST Studio Suite® is a high-performance 3D EM analysis software package for designing, analyzing and optimizing electromagnetic (EM) components and systems.

https://www.3ds.com/products-services/simulia/products/cst-studio-suite/

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